Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

**PAD FUNCTION:**

1. **A1**
2. **B1**
3. **Y1**
4. **A2**
5. **B2**
6. **Y2**
7. **GND**
8. **Y3**
9. **A3**
10. **B3**
11. **Y4**
12. **A4**
13. **B4**
14. **VCC**

**.024”**

**.024”**

**2 1 14 13**

**12**

**11**

**10**

**3**

**4**

**5**

**6 7 8**

**HCT00Y**

**MASK**

**REF**

**Top Material: Al**

**Backside Material: Si**

**Bond Pad Size: .004” X .004”**

**Backside Potential: Isolated or VCC**

**Mask Ref: HCT00Y**

**APPROVED BY: DK DIE SIZE .024” X .024” DATE: 12/14/22**

**MFG: FAIRCHILD THICKNESS .014” P/N: 54HCT00**

**DG 10.1.2**

#### Rev B, 7/1